Stress Induced By Silicon-Germanium Integration in Field Effect Transistors

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Abstract

The integration of high level of stress in field effect transistors is performed through incorporation of intrinsically strained SiGe layers. With the help of COMSOL simulations, we performed two studies addressing the level of stress in the area of interest. In the first case, we analyzed the geometric effects of the SiGe film stress relaxation on the edges. In a second time, we studied the final level of stress as a function of different Ge concentrations in both the channel and the source/drain. We found out that the Ge content in the channel has no impact on the stress induced by the source/drain region.

Figures used in the abstract

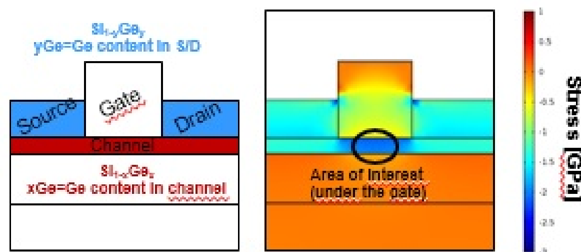

Figure 1: Illustration of the structure with Ge concentration in the channel xGe and in the Source/Drain yGe (left). Mapping of the final stress induced by SiGe in the channel and in the Source/Drain (right).

Figure 2

Figure 3

Figure 4