Void Shape Evolution of Silicon Simulation in COMSOL Multiphysics®

C. Grau Turuelo[1], B. Bergmann[1], C. Breitkopf[1]

[1]Technische Universität Dresden

Abstract

The void shape evolution of silicon is a thermodynamically driven process which leads to a geometrical transformation from cylindrical trenches etched in a silicon wafer to empty spaces in silicon with a spherical or plate shape when those trenches are annealed at high temperature and low pressure conditions as reported in previous experimental publications [1-4]. The applications of this process are framed in the Silicon on Insulator (SOI) devices manufacturing as the insulation layer beneath the electronic devices fabricated by the void shape evolution can reduce the parasitic device capacitances/resistances as well as decrease the insulator area or provide a better heat tolerance thus improving the performance [5, 6].
The surface migration is interpreted by a rearrangement of the surface atoms due to gradients of the Gibbs-Thomson chemical potential as detailed in the Mullins theory of thermal grooving where the chemical potential drives a surface atomic flux which modifies the surface thus provoking a normal velocity that can be calculated [3,4,7]. The development of a theoretical model that uses surface diffusion as the main phenomenon has been carried out by the use of the specialized simulation software COMSOL Multiphysics®. For the execution of this model, custom boundaries EDP equations were programmed to calculate the chemical potential and the velocity of the surface by the adaptation of Mullins' theory equations to the software interface. In addition, the Moving Mesh interface was used for transforming those results in a visual evolution of the simulated surface giving a defined view of the morphological changes in the void shape evolution at different geometries and temperatures. An example of such a model is displayed in (Figure 1).
The simulations were carried out through several temperatures (from 900°C to 1200°C) and different initial cylindrical geometries, by the variation of diameter and length, to examine the post-anneal morphology in order to observe the patterns that this process follows and find reliable relations between the initial and the final geometrical state (more data in the respective poster). The impact of other factors such as pressure or the coalescence of more than one trench is also under development.
As a summary, the shape evolution of a trench patterned silicon substrate results in diverse cavities by varying initial conditions. As described in several studies, the size and the arrangement of the basic trenches are decisive for the transformation process besides the annealing conditions which are, in fact, time and temperature, and the existing pressure values [1-4]. Thus, the prediction of the shape evolution depending on different conditions improves controllability and the feasibility of building new micro-electronic or micro-electromechanical devices such as pressure sensors, transistors or optical devices [8].

Reference

1. I. Mizushima et al.,Empty-space-in-silicon technique for fabricating a silicon-on-nothing structure , Jpn. Appl. Phys. Lett. 77, 3290 (2000)
2. T. Sato et al.,Fabrication of Silicon-on-Nothing Structure by Substrate Engineering Using the Empty-Space-in-Silicon Formation Technique , Jpn. J. Appl. Phys. 43, 12 (2004).
3. K. Sudoh et al., Numerical Study on Shape Transformation of Silicon Trenches by High-Temperature Hydrogen Annealing, Jpn. J. Appl. Phys. 43, 5937 (2004).
4. K. Sudoh et al.,Void shape evolution and formation of silicon-on-nothing structures during hydrogen annealing of hole arrays on Si(001), J. Appl. Phys. 105, 083536 (2009).
5. M. Jurczak et al., Silicon-on-Nothing (SON)—an Innovative Process for Advanced CMOS, IEEE Trans. Electron Devices 47, 2179 (2000).
6. S. Monfray et al., First 80nm SON (Silicon-On-Nothing) MOSFETs with perfect morphology and high electrical performance, 2001 International Electron Devices Meeting, Washington DC, United States, 2 December–5 December 2001, pp. 645-648.
7. W. W. Mullins, Theory of Thermal Grooving, J. Appl. Phys. 28, 333 (1957).
8. T. Sato et al.,Method for fabricating a localize SOI in bulk silicon substrate including changing first trenches formed in the substrate into unclosed empty space by applying heat treatment, United States Patent US 7,507,634 B2, 24 March 2009.

Figures used in the abstract

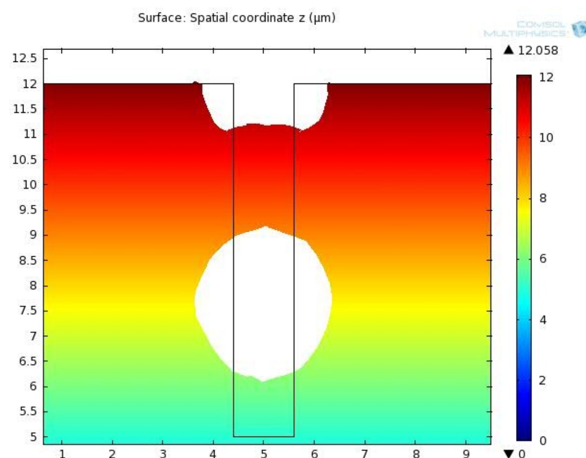

Figure 1: Simulation result at 1100 °C. Initial trench had a radius of 0.6μm and a depth of 7μm