Investigation of a Hybrid Winding Concept for Toroidal Inductors Using 3D Finite Element Modeling

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Abstract

Introduction: The conventional wire wound toroid shown in Figure1 is used extensively in switch mode power supplies in EMC filters and as inductors and transformers. However the space between the windings increases gradually from the inner diameter towards the outer diameter of the core which limits the utilization of the available winding space. This effect increases the resistance and thus the conduction loss of the component [1,2]. To overcome these disadvantages a hybrid winding scheme may be used[3]. The basic idea of the hybrid winding scheme is to cut and bend copper foils into "U" shaped pieces that fit around the toroidal core as shown in Figure 2. To complete the winding the foil pieces are connected through the traces in a printed circuit board (PCB).

Use of COMSOL Multiphysics®: The challenge of predicting the resistance as a function of the frequency of such a complex 3D winding geometry is solved using COMSOL Multiphysics® with the AC/DC Module[4]. The greatest challenge was to create the mesh since eddy currents needs to be considered and the thickness of the foil to the PCB traces vary from 0.5mm to 70µm. A boundary layer mesh with 4 layers and a stretch factor of 2.5 was used. The first layer fitness was set manually to 5µm For the DC resistance simulation a free tetrahedral mesh was used.

Results: In Figure 3 the current density at 100kHz in the foil cutouts and the PCB traces are shown. The 3D model of the hybrid inductor is shown from beneath in order to inspect the PCB traces. Some of the windings and the core are hidden in order to look at the inner part of the winding. From the colors it is easy to see that the current density is highest closest to the core where the current path is shortest and in the places where the width of the foil cutout is lowest. This suggests that the foil cutouts should be angled instead of the PCB traces in order to reduce the resistance.

In Figure 4 the simulated and measured resistance as a function of the frequency is shown. An offset is added to the simulation result to compensate for any static error sources such as imprecise cuts and clearance of the bent foils, all of which is not included in the 3D model

A COMSOL LiveLink™ product for a computer aided design (CAD) program [5] was also used and several simulations were performed in order to investigate the resistance versus the PCB Thickness. The simulation proved that the PCB trace thickness is a bottleneck for high power applications.

Conclusion: The simulation with offset fits the measured results from 10 Hz to 100 kHz which is the common operating frequency range. It is found that the commercially available layer thickness of printed circuit boards is a bottleneck for high power applications. Finally a plot of the simulated current density in the winding reveals that the winding configuration can be optimized which is crucial for performance.

Reference

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Figures used in the abstract

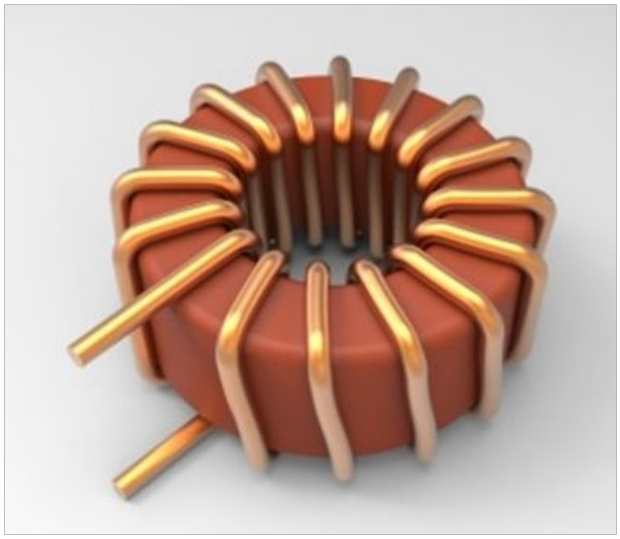

Figure 1

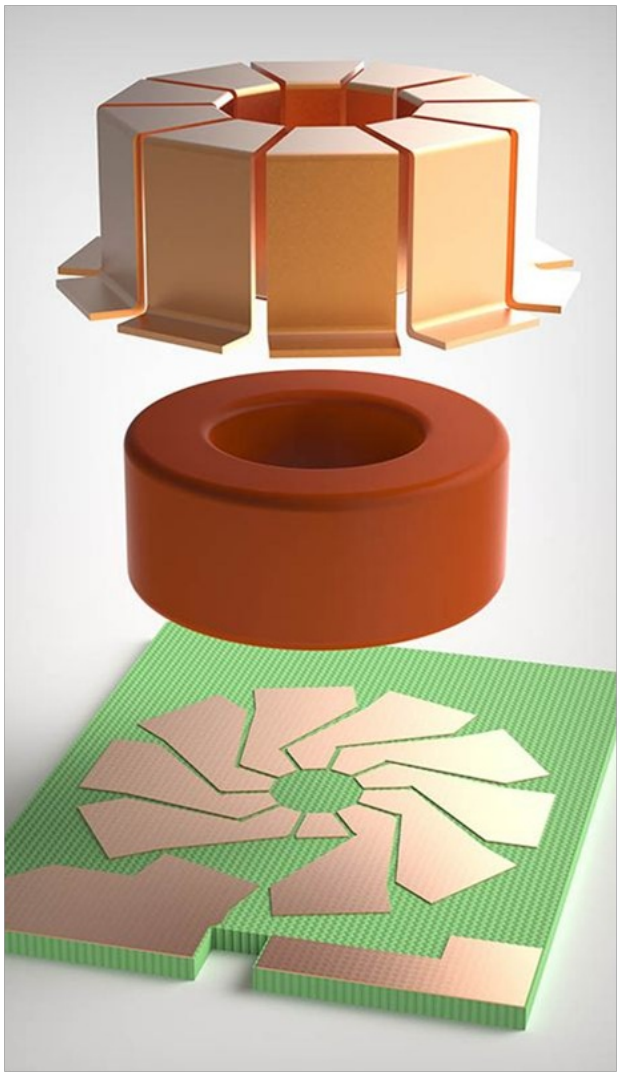

Figure 2

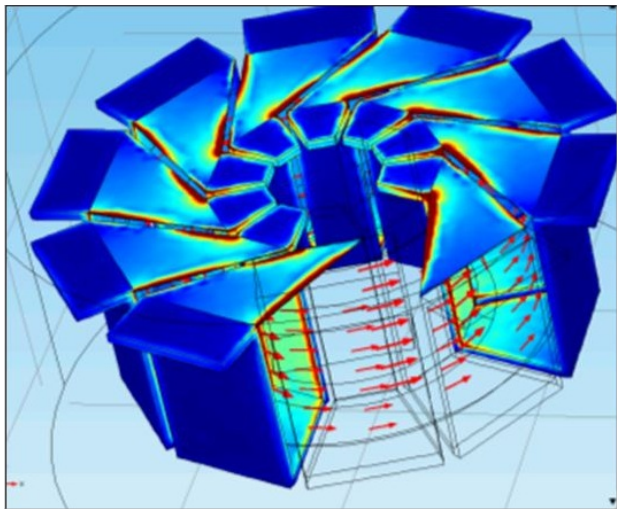

Figure 3

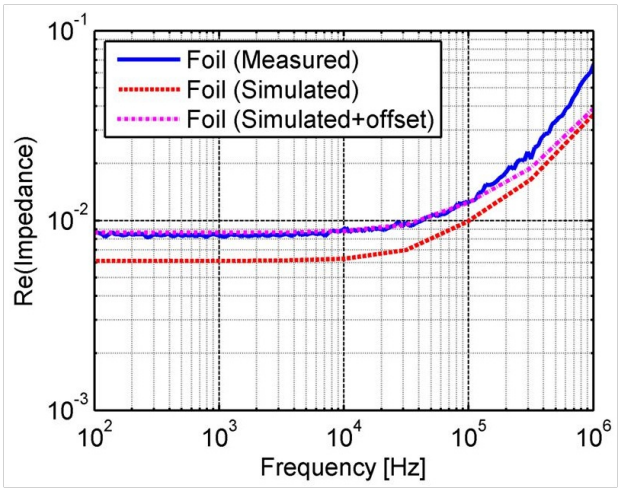

Figure 4