Modeling Internal Heating of Optoelectronic Devices Using COMSOL

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Abstract: In this paper the heat transfer module in COMSOL is utilized to simulate internal heating of an avalanche photodiode due to light-induced current through a resistivity that depends on charge carrier concentrations in the device. Initial tests are done by modeling the heating process on a previously-solved silicon p-n junction as a proof of concept before advancing to a more complicated geometry. Strategies for mapping heterojunction material properties are discussed and estimates for carrier concentrations and current in place of a full carrier model solution are explored. A second model of heat power from current and voltage mapping is presented.

Keywords: Optoelectronics, Joule Heating, Heterojunction Semiconductor, Avalanche Photodiode

1. Introduction

In operation, optoelectronic devices are subject to heating due to environment, incoming light, and resistive heating (Joule heating) due to current flow. It is important to characterize this heating, as the temperature of the device affects the operating parameters of the device and, in extreme cases, heating can even cause failure via compromising dielectric material, melting or migrating of metal contacts, and even dopant migration.

This particular model is focused on the operation of an avalanche photodiode (APD) in exploration of possible failure modes during survivability tests. The most significant heating source in this model is of carrier charges traversing the device, modeled by a forced current subject to a resistivity across the device dependent on charge carrier concentration and mobility. The legitimacy of this model, and an alternative based on voltage drop and current, is finally explored to evaluate the results.

2. Avalanche Photodiode Overview

An APD can be considered the solid-state version of a photomultiplier tube. When placed under a strong reverse bias, incoming light is amplified to create an output of charge pairs greater than the input of photons. This is due to a high electric field multiplication region within the device in which charge carriers are accelerated to a high enough energy to generate additional carriers through impact ionization events. The gain is calculated as the average number of carriers out for each carrier in and depends on the voltage applied to the device.

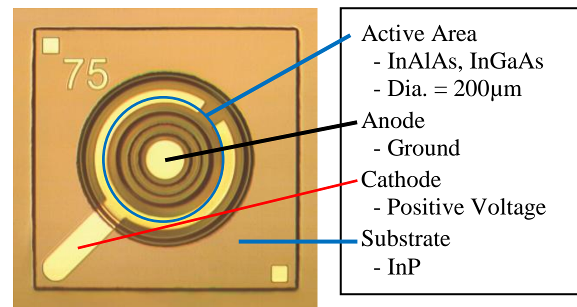

Figure 1. The active side of a Voxtel APD, showing metal contacts. The device is to be illuminated from the back and reverse biased.

The particular device to be modeled is a heterojunction APD constructed of InGaAs and InAlAs layers lattice-matched to an InP substrate. The active area is a disk of 200µm diameter about 3µm thick. The device is actively cooled through thermal contact with a thermoelectric cooler (TEC). Doping densities include heavy doping of 5E18 cm^{-3} or 1E18 cm^{-3} and an intrinsic n-doping of 1E15 cm^{-3}. The geometry of the device modeled will not be discussed in depth in this paper.

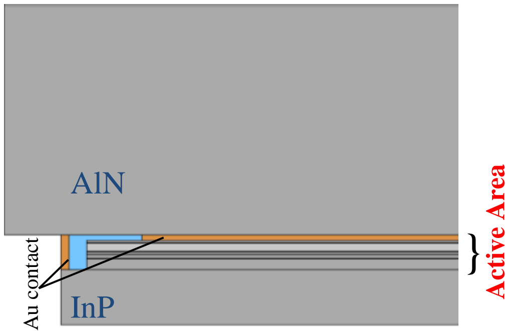

Figure 2. Cutaway of the APD model with substrate and AlN cooling block.

3. Testing with P-N Junction

As a proof of concept, we look at a p-n junction that was provided by COMSOL[1], which we will apply as a solar cell. The model solves for charge carrier concentrations as a Transport of Diluted Species model, and has been solved for various reverse voltages in the range 0-1 V. We map the resistivity of the device as

$$\rho = \left(q\mu_n n + q\mu_p p\right)^{-1} \text{ (eq. 1) } ^2$$

where n and p are the carrier concentrations of electrons and holes, μ is the mobility of each, and q is the elementary charge (1.602E-19 C). Checking Sze figure 3.7 shows that we are within good estimates of resistivity for the charge concentrations of the model.

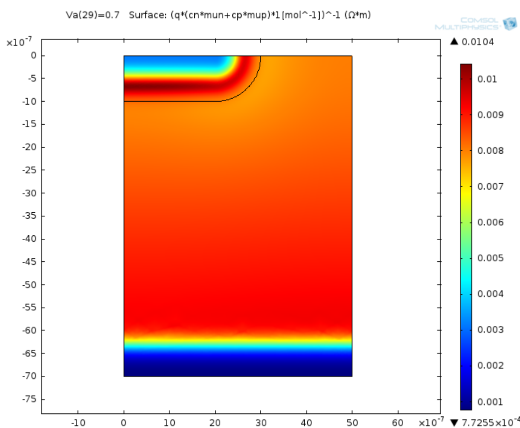

Figure 3. Map of resistivity in p-n junction for $V_r = 0.7$ V.

A high estimate of 1 mA is forced through the device to simulate incoming light and applied equally to the width of the device (5μm) squared. The resistivity of the device (Ω·m) is multiplied by the square of the current density, resulting in a map of the Joule heating due to current flow with units of W/m^3. This is the incoming heat energy.

The equation for heating is given as

$$\rho C_p \boldsymbol{u} \cdot \nabla T = \nabla \cdot (k\nabla T) + Q \text{ (eq. 2)}$$

where ρ, C_p, and k are the density, heat capacity, and thermal conductivity of the material (silicon in this junction), T is the temperature, and Q is the incoming heat energy found in the above paragraph. The heat transfer module is used to apply Q across the whole of the device and a simplified boundary condition of room temperature (293 K) across one side is added.

The model stabilizes with a peak temperature of 295.6 K, a believable value for 1 mA. This gives a proof of concept for resistance heating as a function of charge carriers, though we have obviously ignored the horizontal additions to current in this particular model.

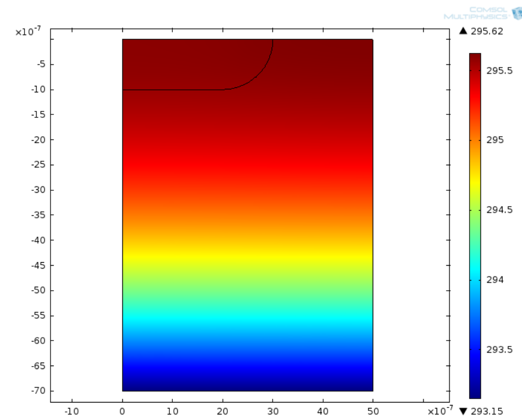

Figure 4. Final temperatures with 1 mA forced at 0.7 V.

4. Initial Conditions and APD Properties

4.1 Model Definitions

In order to easily handle the many properties of each of the heterojunction layers in an organized way, properties are defined using Variables that apply specific domains within the geometry. In this way p, n, and mobility values are defined to correspond to the material in each layer and the depletion region (discussed in section 4.3) can easily be set to variable charge densities.

4.2 Mobility

The mobility of a semiconductor is inversely proportional to the temperature as T increases around 300 K. In order to account for this we fit

a linear relationship to a mobility vs. temperature graph in the region of operation. An accurate room-temperature value for InGaAs, previously found by our experiments, is used and subtracted by $\nabla T * \frac{\partial \mu}{\partial T}$ as estimated from the mobility graph.

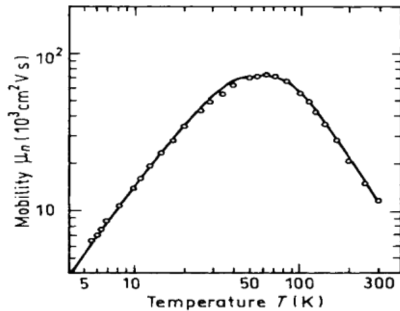

Figure 5. Mobility vs. Temperature for InGaAs, showing inverse correlation with temperature at 300K.[3]

4.3 Depletion and Charge Carriers

During operation, a large portion of the device becomes depleted due to a region of high electric field, effectively removing the charge carriers and thus increasing the resistance in the area. Because I was unable to complete a full charge-carrier model using COMSOL, an estimate for concentration was done by using the results of a previous 1-d simulation of the geometry in Sim Windows.[4]

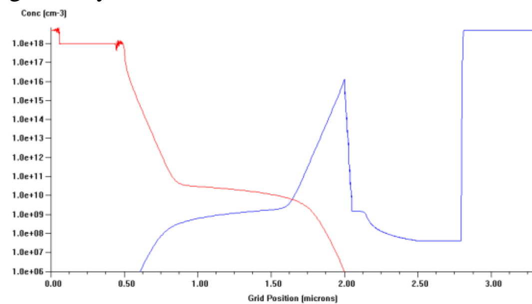

Figure 6. SimWindows simulation of charge carriers, with a log scale on the y-axis.

The output of this model confirms that charge density is about equal to dopant levels outside of the depletion region, and an average of the highly non-linear output is taken to estimate the remaining carrier concentration inside the depletion region.

4.4 Meshing

It is important that the mesh fit properly to calculate the physics on distance scales important to the geometry. The smallest domains are 500 Å thick and need to have multiple points to characterize physics within the layer, but the larger substrate and block do not need the 10 nm resolution of smaller layers.

The Distribution feature is used to define 5 points across the small thicknesses and 400 points across layers to ensure horizontal resolution. The active area is then mapped with a square mesh grid to guarantee multiple vertical points throughout the layer. A free triangular mesh is used throughout the rest of the model to align with the fine mesh in the active area but expand away to reduce the necessary points for calculation.

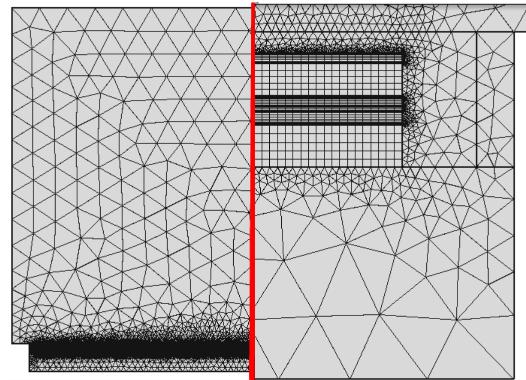

Figure 7. Left: an overview of the entire mesh geometry. Right: a close-up of mesh where the active area meets the substrate (lower), dielectric, and AlN block (above).

4.5 Heating Boundary Conditions

The initial temperature of the device is 293.15 K, the default room temperature in COMSOL. Surface-to-Ambient radiation is set on the substrate edge to simulate contact with air and an estimated emissivity of 0.5 used.[5] The far edge of the AlN block is set to the TEC controlled temperature of 250 K. All of the material properties important to heat transfer (heat capacity, etc.) are defined per domain in the same manner as in 4.1.

5. Heating Process

The simulation will follow lab conditions, in which a pulsed 1550 nm laser is fired into the APD with a varying peak power. A typical strong signal is a peak power of 10W over a 3 ns

pulse, repeated at 10 Hz. Previous characterization shows that our devices have a responsivity of 1 Ampere of current per Watt of incoming light. Using a gain of 10 (a typical device setting) the peak power will result in $1\frac{A}{W} \cdot 10\, W \cdot 10 = 100A$ current pulses, spread across the active area diameter of 200µm. A first-order approach simplifies the pulsed input to an average power using 100ms / 3ns.

The resistivity due to our charge concentration, ρ, is mapped and multiplied by the square of average current, 3mA applied over $\pi(100\mu m)^2$, resulting in the heating map Q. Equation 2 is used through the heating module in COMSOL in conjunction with boundary conditions explained in 4.5, and the result is a heat map that peaks at 252 K, just over 2 degrees warmer than the TEC set temperature.

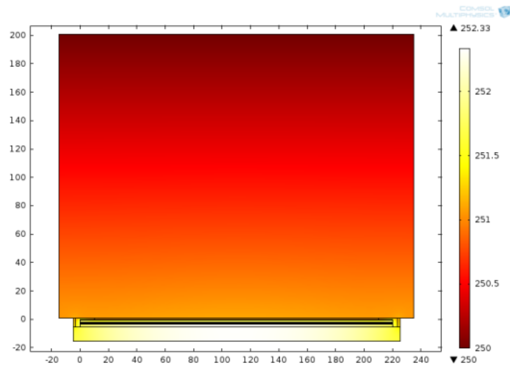

Figure 8. Overview of heating in the device with 10W peak power incoming.

This is such low heating that an extension is performed on the solver to model incoming peak power in 10 W steps from 10-100 W. The result of the 100 W peak input is a peak temperature of 486 K. Graphing the temperatures along the edge of the active area shows that T seems to remain fairly constant across the device until, in larger incoming powers, the high-resistivity depletion region begins to become noticeably hotter than the rest of the device.

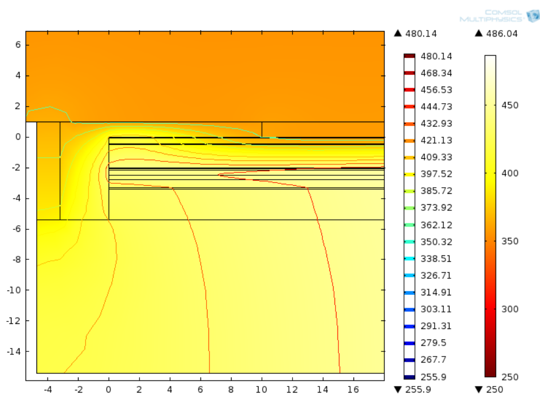

Figure 9. Active area and substrate under 100 W peak power illumination.

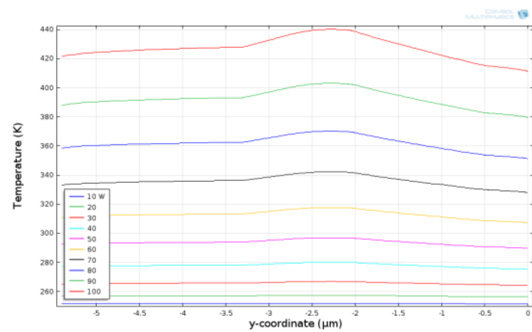

Figure 10. Temperature along edge of active area for different incoming powers.

6. P = I·V and Time Dependence

There are some errors in the resistivity model we have just outlined. In the depletion region, where most of the voltage change occurs, the carriers will reach their saturation velocity. At this point, the mobility (of units cm2/V·s) will continually decrease given the constant saturation velocity of cm/s but an increasing value of V/cm as more potential is applied.

Another strategy for Joule heating in the device is to use the power derived from the forced current and multiply it by the potential drop. As each charge carrier in the current traverses the potential work is done on the charge, and this energy in the IV model is all assumed to go into heating the device.

To model this, the same properties and boundary conditions described previously are used, but change the input heating Q. Again, forced currents ranging from 100 A to 1 kA are used. As in an idealized p-n junction, it is assumed that all voltage drop will occur in the

depletion region, and select that as our domains for heat input. A voltage change of 50 V is estimated, which is an estimate for M=10 settings, and I·V is applied as a total power for the heat source of the model. This will apply the heating equally across the depletion regions.

An initial test utilizing the same average current technique to deal with the time-dependency of light input led to a result with no heating, so a time-dependent model was performed over 100 ns, with 10 W light current induced for the first 3 ns. The result was a maximum temperature of 390 K in the active region, as shown on figure 11, and then decreasing as heat was dissipated. Running the model to 100 ms showed that the temperature would drop back to base at the time of the second light pulse. Thus, 390 K is the hottest point that the device will hit at 10 W incoming peak power. Raising the incoming light to 100 W peak led to an astounding 1200 K peak temperature, probably resulting in failure of dielectric in the device. A similar time-dependent model with the resistivity model was not converged as of the writing of this paper.

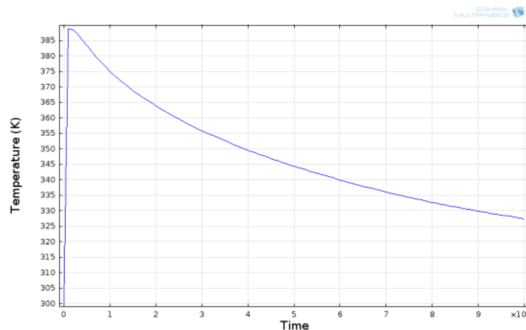

Figure 11. Temperature at a point in the active area with respect to time. The light pulse induces current for t <= 3 ns.

7. Conclusions

Our devices are subject to 450 K in order to cure the encapsulating dielectric material, which has a glass transition temperature of 650 K. Temperatures lower than these should serve as definite safe points, and above may mean failure in the dielectric material. Prolonged exposure at temperatures in this range may lead to significant dopant migration, but generally 650 K can be used as a safe cutoff.

With the resistivity model, tests heated to just about the curing temperature with our highest incoming light measurements. This means no failures are expected from the model. However, utilizing the IV model, we were able to see that heating occurs several orders of magnitude higher in the peak of a time dependent model compared to the average heating, and this is the most likely time when the device will fail (if failure conditions are reached).

Future tests with the resistivity model should include a calculation of a mobility value from the saturation velocity and voltage characteristics. They should also include a more advanced estimation in the depletion layer, if not a full convergence model of charge carrier distribution and electric field, as done in the p-n junction example. It would also be ideal to incorporate the absorbed light into a current flow in the charge carrier model via a carrier generation term, and to show how heating across the device evolves on very short time scales.

New work with an I·V model would be more complete if the voltage was properly mapped over the depletion region, rather than estimated to be equal across it. This could be calculated from a solved carrier model, described in the paragraph above, and compared to the expanded resistivity model.

8. References

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9. Acknowledgements

The author would like to thank Dr. Andrew Huntington for his research guidance and advice. The author would also like to thank Dr. David Barsic for his guidance and review, and Tim Kilian for his artistic input on the affiliated research poster.