

CdS Thin Film Transistor Threshold Voltage Shift Investigation

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Abstract

A threshold voltage shift of CdS Thin Film Transistor is studied using COMSOL's semiconductor module. Drift-diffusion (DD) simulation model is used in which the basic equations used are similar to those used for a single-crystal device except that traps and defects are included in the model. It is assumed that traps due to grain boundaries are uniformly distributed throughout the film. Both exponential and Gaussian trap distributions are introduced in the simulation. The threshold voltage shift was accounted for by bulk traps in the CdS active material and interface traps and charges at the interface between the CdS channel and HfO₂ insulator interface. The quantity of the traps and interface charges are determined by matching the simulation I-V curves with experiment.