Chip Drop after Silver Sintering Process

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Abstract: Since a couple of years, sintering becomes more and more important for power electronics. To press a semiconductor under high temperature in silver paste on a substrate promises benefits for durability. Tests with semiconductors of different thickness expose some problems. After the cool down, some of them fall slightly from the substrate. Stress in the boundary layer, caused by different expansion coefficients, is probably the reason for this effect. To describe the reasons and mechanisms of these phenomena, some simulations with different programs were started. The aim is to understand and specify the effects of different thermal expansion coefficients in such a thermal stack.

Keywords: Sintering Process, Chip Drop, Stress.

1. Introduction

In power electronic devices, the most common method to connect the drain of a semiconductor with the substrate is a soldering process (**figure 1**). To increase the reliability of the chip to substrate connection, sintering became more and more importance.

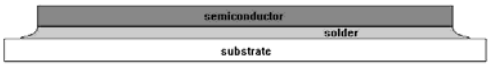

Figure 1: typical soldering stack

During the sintering process [2,3], a semiconductor will be pressed under high temperature in silver paste on a substrate. Normally, the result of this process is a permanent joint between the substrate and the semiconductor (**figure 2)**.

Figure 2: typical sintering stack

In our case, the semiconductor chips lose their joint after the cooling down phase. We decided to examine this effect with two different tools. A comparison between COMSOL and ANSYS has been carried out.

To understand the mechanism behind this aspect, it is necessary to take a look at the mechanical stress.

For the simulation of the stack, the parameters and boundary conditions must be well-known. Also the dimensions of the stack and the governing equations have to be noted.

2. Suhir´s model

Different materials have different expansion coefficients. The different expansions in a thermal stack lead to stress in the structure. For the stress distribution and the resulting coving has Suhir developed models [1, page 205 ll.]. The Suhir model exists for bimaterial and trimaterial assemblies (**figure 3**) and extends the well known Timoshenko model [1, page 197 ll.].

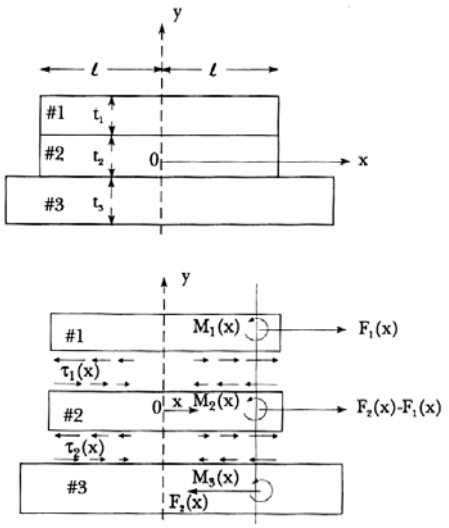

Figure 3: Stress analysis model for Suhir´s analysis

The forces and moments shown in figure 3 results from the different thermal expansion coefficients of the three different materials and appears when the temperature is lowered from the stress-free die-attach temperature.

In the Suhir model, it is necessary that the displacements $u_1^-(x)$ of the lowest lamella of the

first layer (chip) be equal to the displacements $u_2^+(x)$ of the top lamella of the second layer (silver) and so on. It leads to:

(1) $u_1^-(x) = u_2^+(x)$ and $u_2^-(x) = u_3^+(x)$

This displacements, also shown in figure 3 are given by:

(2)
$$u_1^-(x) = \alpha_1 \Delta T x - \lambda_1 \int_0^x F_1(\zeta) d\zeta + \kappa_1 \tau_1(x) + \frac{t_1}{2} \int_0^x \frac{d\zeta}{r(\zeta)}$$

(3)
$$u_2^+(x) = \alpha_2 \Delta T x + \lambda_2 \int_0^x F_1(\zeta) - F_2(\zeta) d\zeta - \kappa_2 \tau_1(x) - \frac{t_2}{2} \int_0^x \frac{d\zeta}{r(\zeta)}$$

(4)
$$u_2^-(x) = \alpha_2 \Delta T x + \lambda_2 \int_0^x F_1(\zeta) - F_2(\zeta) d\zeta + \kappa_2 \tau_2(x) - \frac{t_2}{2} \int_0^x \frac{d\zeta}{r(\zeta)}$$

(5)
$$u_3^+(x) = \alpha_3 \Delta T x + \lambda_3 \int_0^x F_2(\zeta) d\zeta - \kappa_3 \tau_2(x) - \frac{t_3}{2} \int_0^x \frac{d\zeta}{r(\zeta)}$$

Where:

$\lambda_i = (1-\nu_i)/E_i t_i$ and $\kappa_i = t_i / 3G_i$, $i = 1,2,3$ are axial and interfacial compliances for the three layers

$F_i =$ in-plane forces acting on the various layers, $F_i(x) = \int_{-l}^x \tau_i(\zeta) d\zeta$

$\tau_i =$ shearing stress

$t_i =$ thicknesses of each layer

$E_i =$ Elastic modules

$G_i =$ shear modules, $G_i = E_i / 2(1+\nu_i)$

$\nu_i =$ Poisson´s ratio

$\alpha_i =$ thermal expansion coefficients

$l =$ half-length of the structure

$r =$ radius of curvature of the composite structure

$\Delta T =$ melting point – given temperature

In the equations 2-5, the thermal expansion is given by the first part; the forces find her expressions in the second terms. The inconsistent shearing forces in the direction to the interface are represented in the third part and the final terms results from the bending of the structure.

The forces $F_i(x)$ and the radius $r(x)$ can be set in relationship on the basis of the rotational equilibrium condition from figure 3. With $M_i(x) = -D_i / r(x)$ and $D_i = E_i t_i^3 / 12(1-\nu_i^2)$ we can define:

(6)
$$\frac{t_1+t_2}{2} F_1(x) + \frac{t_2+t_3}{2} F_2(x) = M_1(x) + M_2(x) + M_3(x)$$

If we say $\tau_1(x)$ and $\tau_2(x)$ coincide, we can reduce the equation to:

(7) $$\tau(x) = k \frac{\Delta\alpha \Delta T}{\lambda \cosh kl} \sinh kx$$

The eigenvalue is $k = \sqrt{\lambda / \kappa}$, the axial compliance is:

$$\lambda = \lambda_1 + \lambda_3 + \lambda_{13} = (1-\nu_1)/E_1 t_1 + (1-\nu_3)/E_3 t_3 + t^2/4D$$

and the interfacial compliance is:

$$\kappa = \kappa_1 + 2\kappa_2 + \kappa_3 = t_1/3G_1 + 2t_2/3G_2 + t_3/3G_3$$

t ist the total thickness of the stack and D the total flexural rigidity $D = D_1 + D_2 + D_3$. The gap between the thermal expansion coefficients is $\Delta\alpha = \alpha_3 - \alpha_1$. The shear stress (equation 7) can be solved, if we aspect that $\tau_0 = 0$ and $F(l) = 0$. The curvature of the structure becomes:

(8) $$\frac{1}{r(x)} = \frac{t \Delta\alpha \Delta T}{2\lambda D} \left(1 - \frac{\cosh kx}{\cosh kl}\right)$$

Normal stresses find her maximum at the interfaces and will be, on the bottom of the chip:

(9) $$\sigma_{1b} = \frac{\Delta\alpha \Delta T}{\lambda t_1} \left(1 + 3\frac{t D_1}{t_1 D}\right)\left(1 - \frac{\cosh kx}{\cosh kl}\right)$$

And on the top of the chip:

(10) $$\sigma_{1t} = \frac{\Delta\alpha \Delta T}{\lambda t_1} \left(1 - 3\frac{t D_1}{t_1 D}\right)\left(1 - \frac{\cosh kx}{\cosh kl}\right)$$

The peeling stresses are due to forced bending of the stack despite differences in flexural rigidity of the components. The differences in adherent thickness and flexural rigidities $\mu = (t_3 D_1 - t_1 D_3)/2D$ lead to:

(11) $$p(x) = -\frac{\mu}{\kappa} \Delta\alpha \Delta T \frac{\cosh kx}{\cosh kl}$$

3. Problem

We used a stack with the following parameters. The first layer is pure copper with a thickness of 800µm. The second layer is pure silver with a thickness of 30µm. The last layer is pure silicon with a thickness of 70µm. We have a temperature gap of 200 Kelvin and a radius of 4,5mm (**figure 4**). The material parameters are shown in table 1.

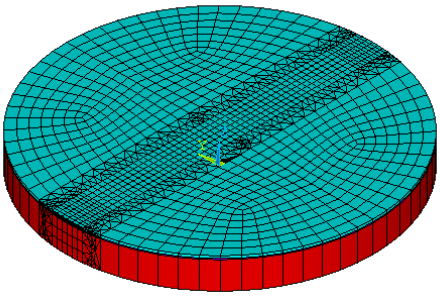

Figure 4: Thermal stack

We will take a look at the mechanical stress and we have to select the correct method to solve this problem.

4. Methods

4.1 Numeric of Suhir´s model

First, we solve the problem for the interlayer between the silver layer and the chip with Suhir´s method (**figure 5**). We use the equations mentioned in chapter two (**equation 9,10,11**)

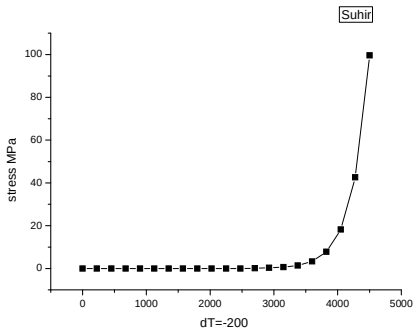

Figure 5: Numerical solution for S_{xz}, Suhir

It must be mentioned that the thickness of the connection layer does not enter into the equations correctly. In Suhir´s model, the thickness of the connection layer is negligible compared to the thickness of the other layers.

4.2 FEM

First we use ANSYS to take a look at the differences between a 2-dimentional axially symmetric model and a 3-dimentional model. The differences between both models are negligible (**figure 6, 7**).

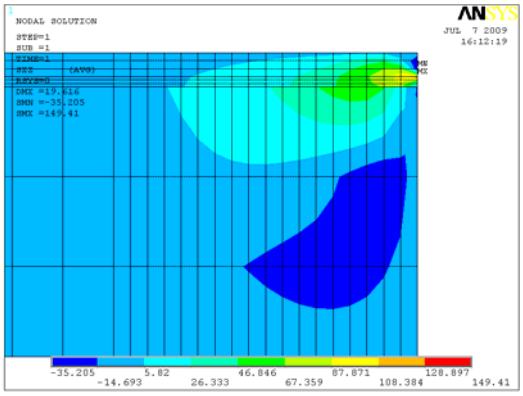

Figure 6: Shear stress, S_{xz}, 3D-model

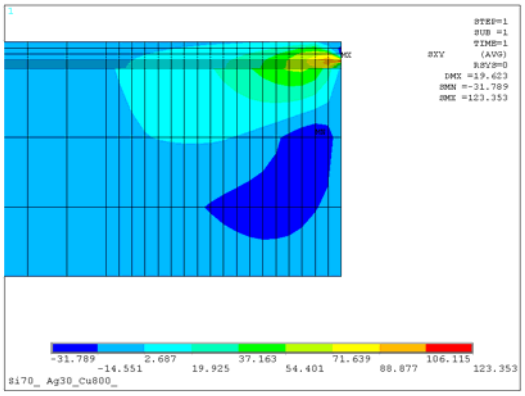

Figure 7: Shear stress, S_{xz}, 2D-axially symmetric

We can not see great differences between the 3-dimentional and 2-dimentional axially symmetric model, even though we take a closer look over all stress components. We can see that the graphs of the different components almost lie on top (**figure 8**).

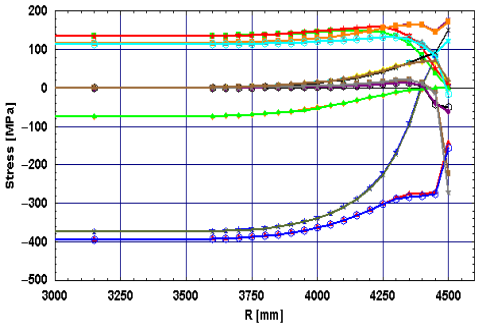

Figure 8: Stress, 3D and 2D-axially symmetric

To compare COMSOL and ANSYS, we use the 2D axially symmetric model, because no significant difference to the 3D model was noticed. We compare the z-displacement in both FEM-tools with Suhir´s model (**figure 9**).

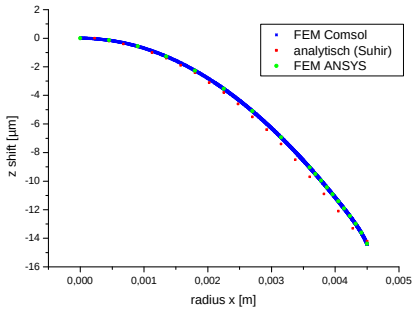

Figure 9: Z-displacement for ANSYS, COMSOL and Suhir

Between the FEM-models and the Suhir model, you can see a small deviation. The graphs of the FEM-programs are approaching the same.

For the shear stress, in both simulation tools we find a maximum (**figure 6, 7, 10, 11**).

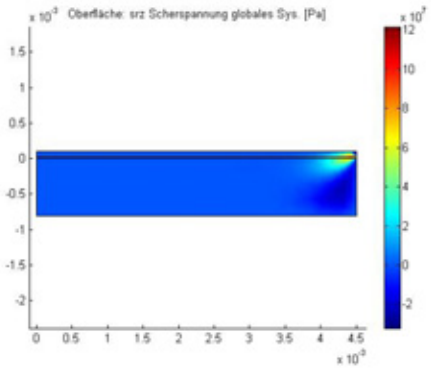

Figure 10: Shear stress with COMSOL

Figure 11: Maximum of the shear stress, COMSOL

It is located between the silver layer and the chip, near the maximum of the radius.

After all, we have made a variation of the thickness of the chip with COMSOL and take a look at the z-displacement (**figure X1**). We solve variants of the thickness with 70, 140, 250 and 460µm.

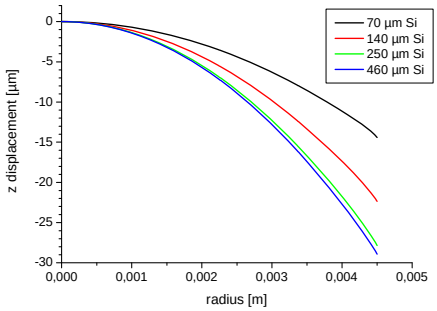

Figure X1: Z-displacement in dependence on the chip thickness

We can see, with increasing the thickness of the chip, the gap between the z-displacements is smaller.

5. Discussion and conclusions

A FEM analysis can show more details than a numeric model. This is not a new idea. Important for us is that we do not need much more time for a COMSOL analysis than for a analytical simulation with Suhir´s model. With some modifications based on Mathlab, we have reduced the simulation time significantly.

The explored maximum near the edge of the silver layer may be partly responsible for the chip drop. Without a FEM-tool this maximum is almost impossible to discover. The variation of the thickness of the chip shows no major impact for the stress at thicker chips. So the influence of

the thickness of the chip is smaller than thought, at least for thick chips

In our institute, COMSOL is a new Program, so it was necessary for us to know, what strengths it offers. The comparatively between COMSOL and ANSYS showed only little differences in the opportunities.

6. References

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7. Appendix

Table 1: Material parameters

Material	Poisson ν	Elastic modul	CTE
Si	0,25	161 GPa	3 ppm/K
Ag	0,3	60 GPa	19 ppm/K
Cu	0,33	125 GPa	16 ppm/K